Fig. 1

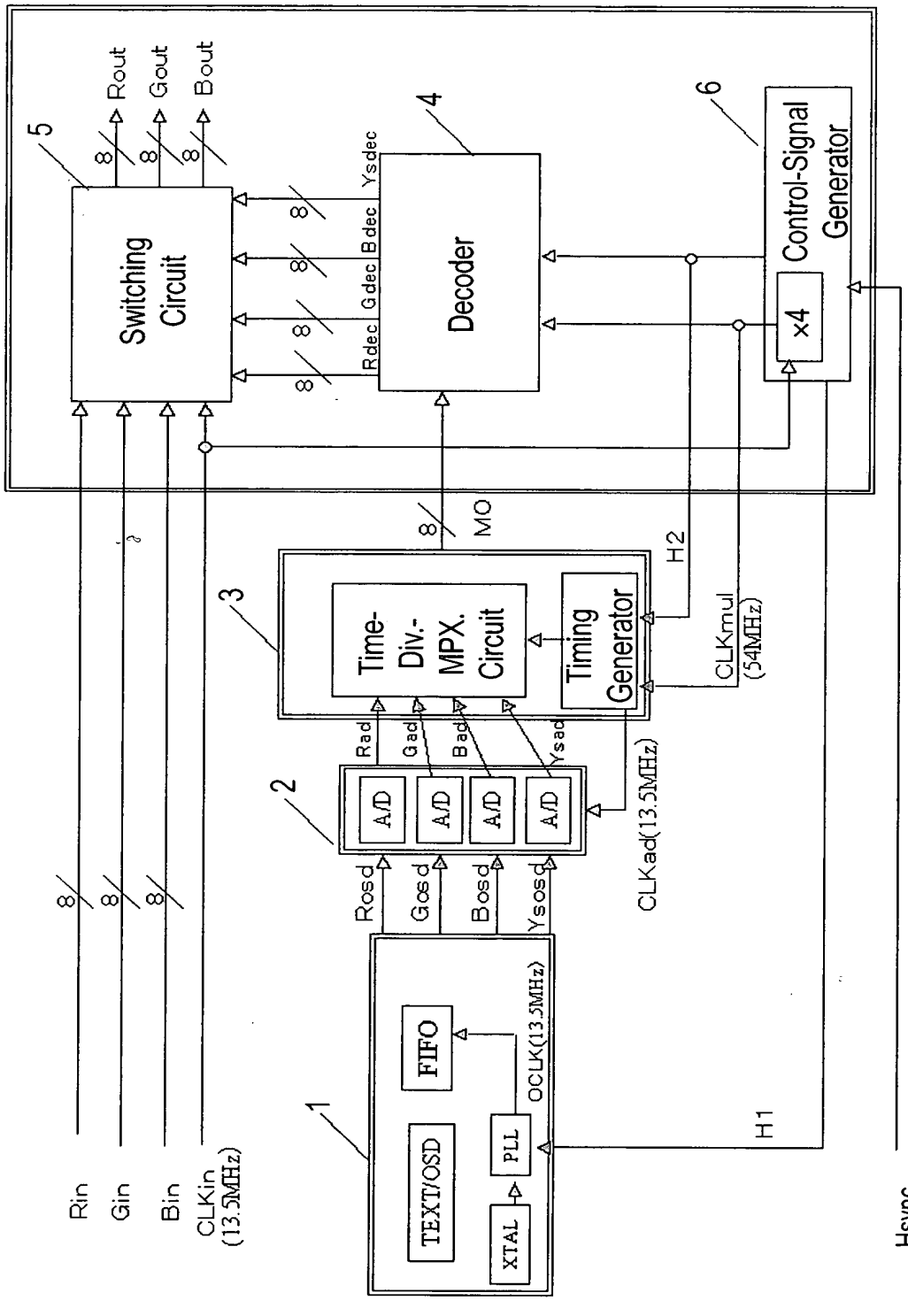

Rout
Gout
Bout
5
Switching Circuit
Ysdec
Bdec
Gdec
Rdec
4
Decoder
6
Control-Signal Generator
x4
8
MO
H2
3
Time-Div.-MPX. Circuit
Timing Generator
CLKmul (54MHz)
Rad
Gad
Bad
Ysad
2
A/D
A/D
A/D
A/D
CLKad(13.5MHz)
Rosd
Gosd
Bosd
Ysosd
1
FIFO
TEXT/OSD
PLL
XTAL
OCLK(13.5MHz)
H1
Rin
Gin
Bin
CLKin (13.5MHz)
Hsync

Fig. 2

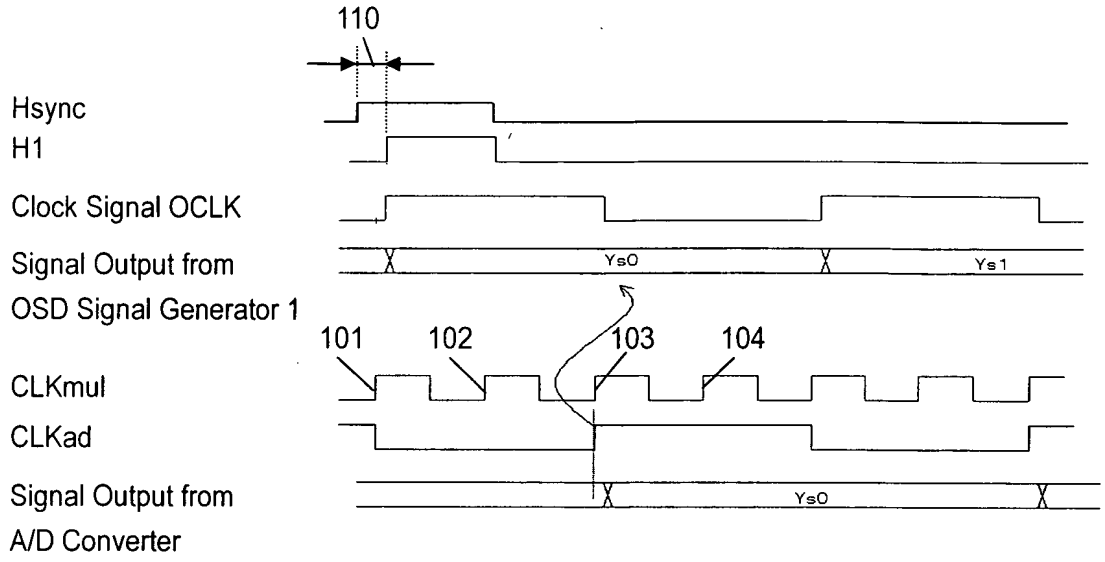

110
Hsync
H1
Clock Signal OCLK
Signal Output from
OSD Signal Generator 1
YsO
Ys1
101
102
103
104
CLKmul
CLKad
Signal Output from
A/D Converter
YsO

Fig. 3

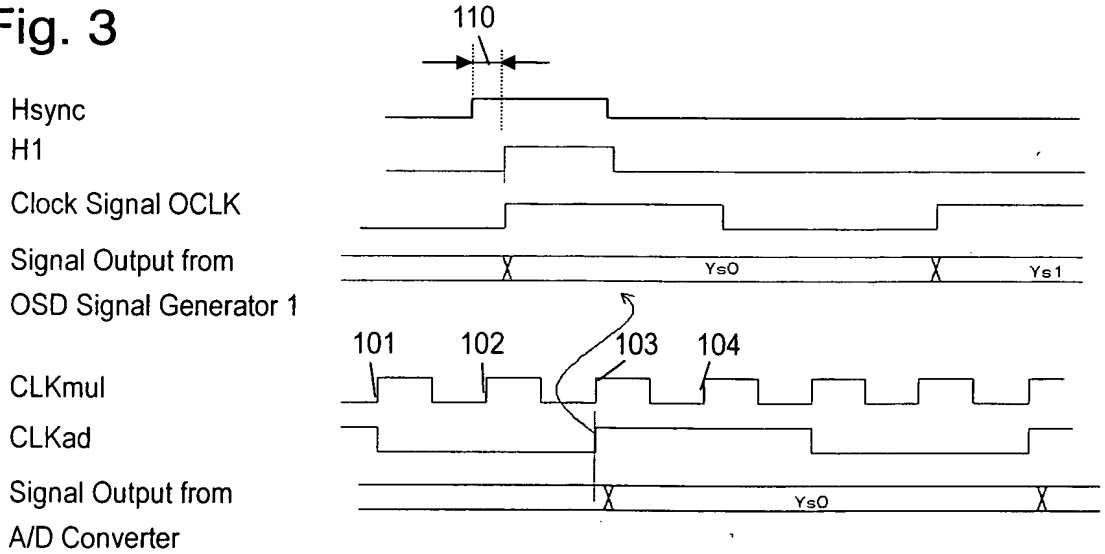

110
Hsync
H1
Clock Signal OCLK
Signal Output from
OSD Signal Generator 1
YsO
Ys1
101
102
103
104
CLKmul
CLKad
Signal Output from
A/D Converter
YsO

Fig. 4

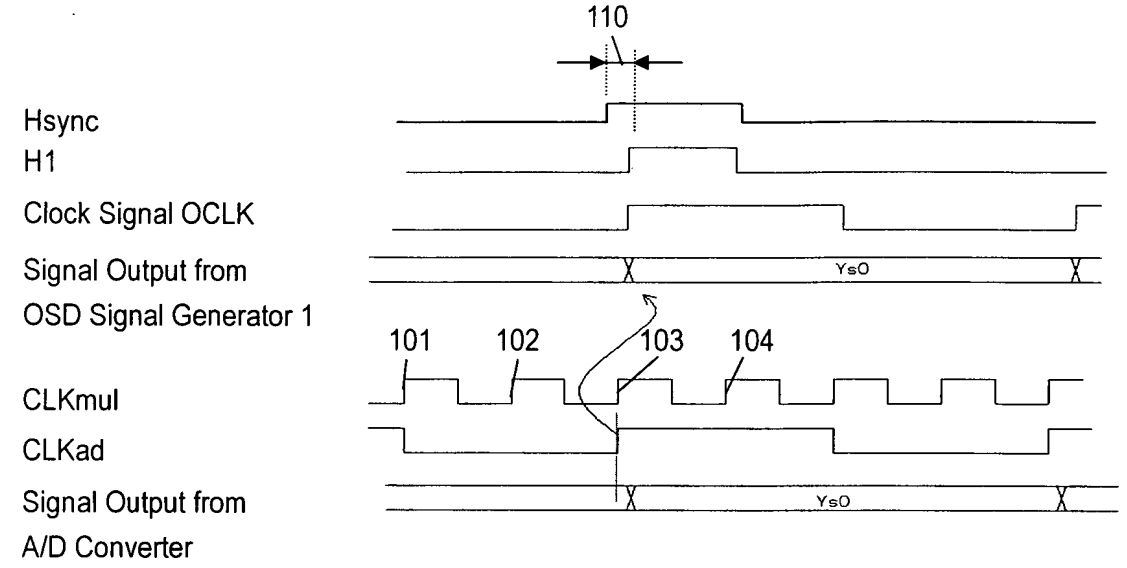

110
Hsync
H1
Clock Signal OCLK
Signal Output from
OSD Signal Generator 1
YsO
101
102
103
104
CLKmul
CLKad
Signal Output from
A/D Converter
YsO

Fig. 5

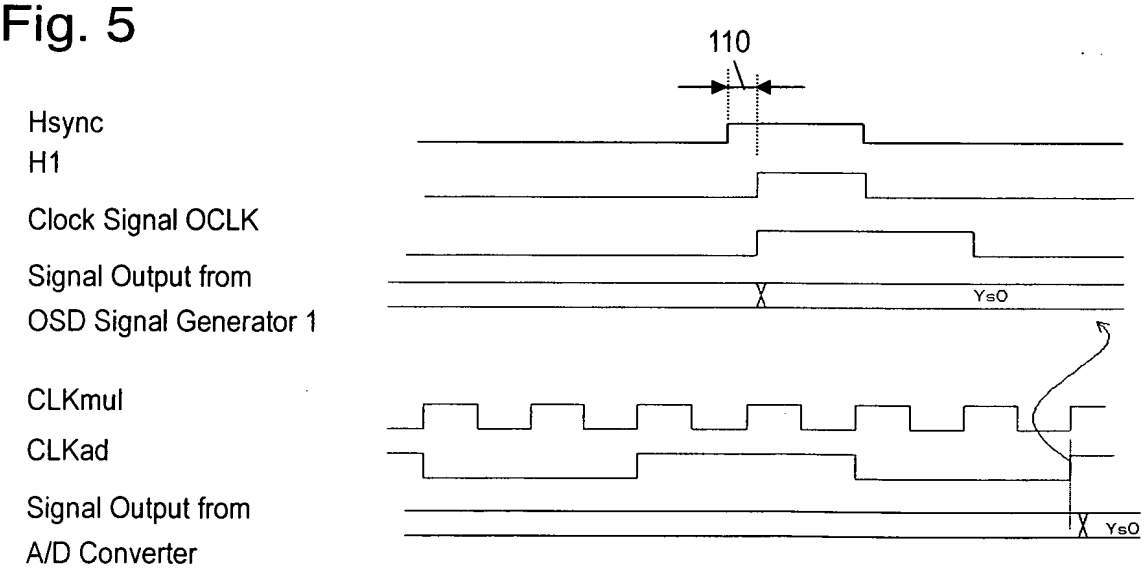

110
Hsync
H1
Clock Signal OCLK
Signal Output from
OSD Signal Generator 1
YsO
CLKmul
CLKad
Signal Output from
A/D Converter
YsO

Fig. 6

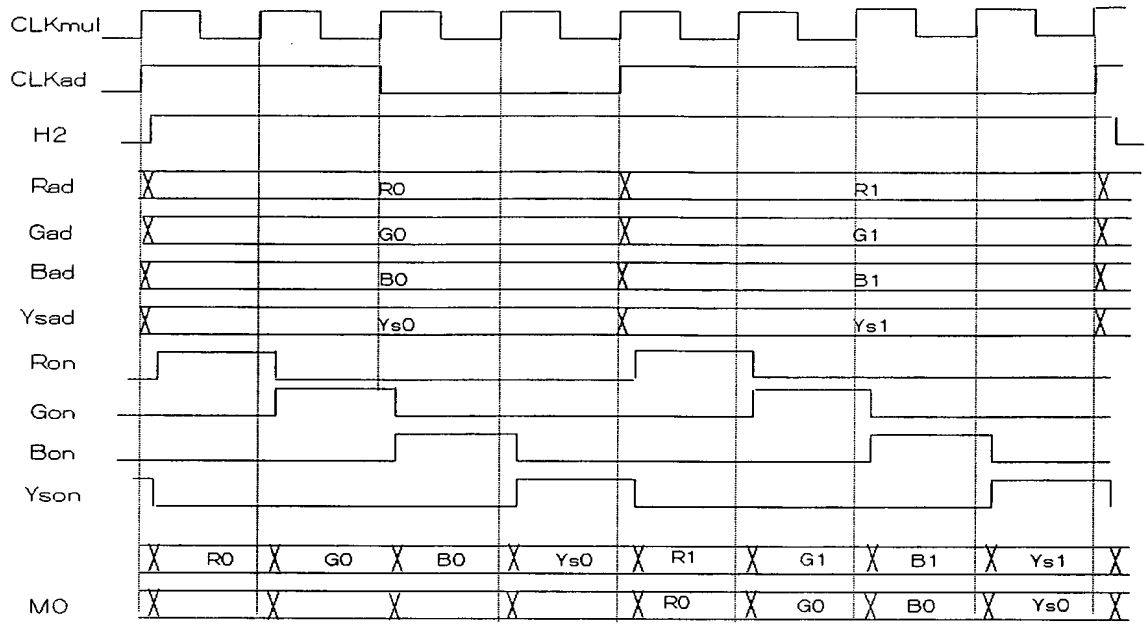
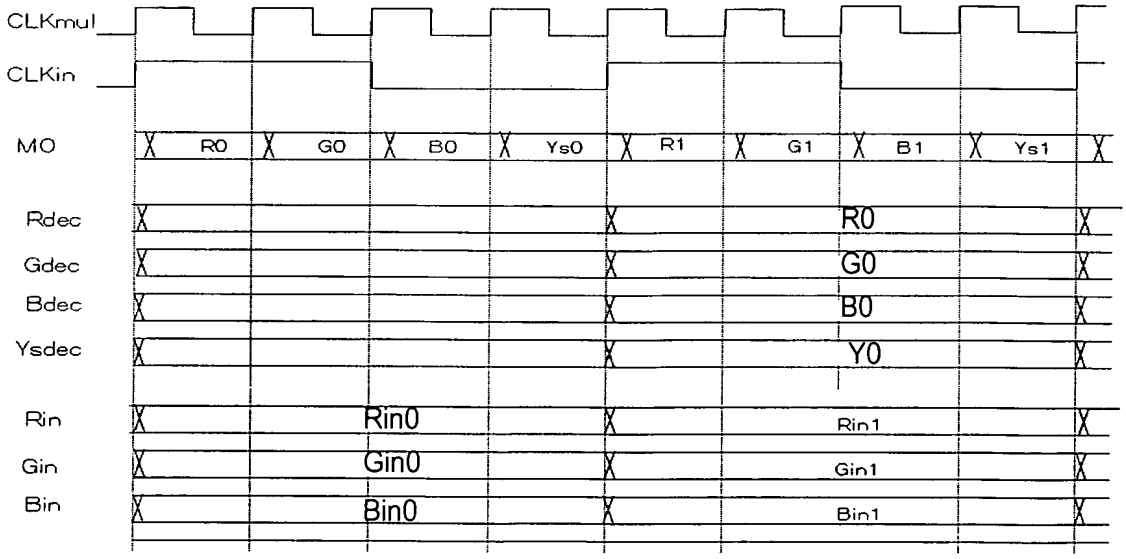

CLKmul
CLKad
H2
Rad
Gad
Bad
Ysad
Ron
Gon
Bon
Yson
MO
R0
G0
B0
Ys0
R1
G1
B1
Ys1

Fig. 7


CLKmul
CLKin
MO
Rdec
Gdec
Bdec
Ysdec
Rin
Gin
Bin
R0
G0
B0
Y0
Rin0
Gin0
Bin0
Rin1
Gin1
Bin1

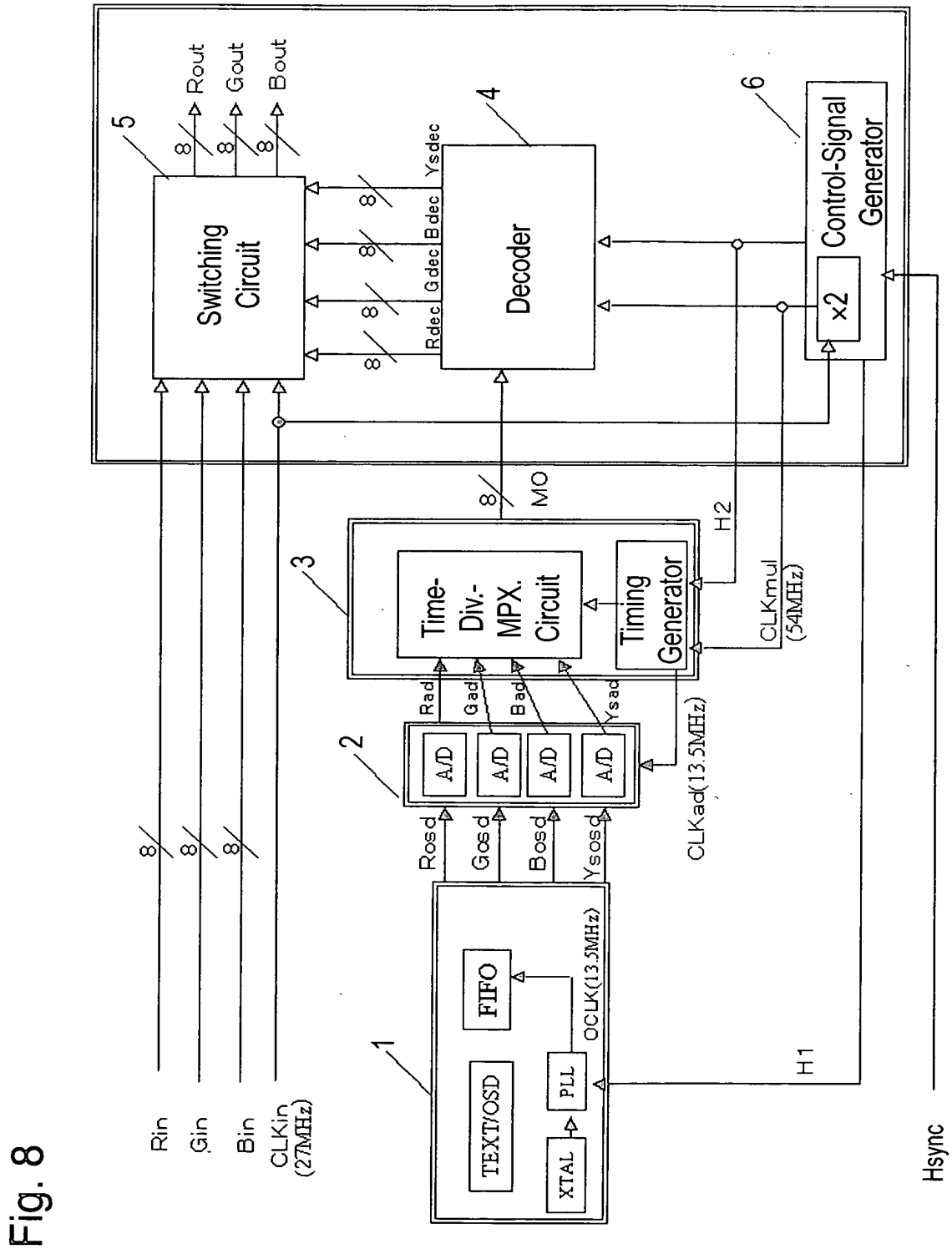

Rout
Gout
Bout
5
Switching Circuit
Ysdec
Bdec
Gdec
Rdec
4
Decoder
6
Control-Signal Generator
x2
MO
H2
3
Time-Div.-MPX. Circuit
Timing Generator
CLKmul (54MHz)
Rad
Gad
Bad
Ysad
2
A/D
A/D
A/D
A/D
CLKad(13.5MHz)
Rosd
Gosd
Bosd
Ysosd
FIFO
OCLK(13.5MHz)
1
TEXT/OSD
PLL
XTAL
H1
Rin
Gin
Bin
CLKin (27MHz)
Hsync

Fig. 8

Reference Numerals

1 OSD Signal Generator
2 A/D Converter
3 Time-Division-Multiplexing Circuit
4 Decoder
5 Switching Circuit
6 Control-Signal-Generator